WHAT IS CLAIMED IS:

1. A synchronous semiconductor memory device operating like a static memory, comprising:

a plurality of dynamic memory cells arranged in rows and columns;

signal input circuitry taking in an external operation control signal in synchronization with a basic clock signal, and producing an internal operation instructing signal;

row select circuitry for selecting, when activated, a row of the memory cells in accordance with an external row address signal;

column-related circuitry for selecting, when activated, a column of the memory cells in accordance with an external column address signal, and performing data access to a selected column; and

control circuitry operating for activating and deactivating sequentially said row select circuitry and said column-related circuitry in a predetermined sequence in accordance with a first internal operation instructing signal provided from said signal input circuitry, for inhibiting deactivation of said row select circuitry to maintain said row select circuitry in an active state in accordance with a second internal operation instructing signal provided from said signal input circuitry, and for deactivating said row select circuitry maintained in the active state in accordance with a third internal operation instructing signal provided from said signal input circuitry.

2. The synchronous semiconductor memory device according to claim 1, wherein

said external operation control signal includes a write instructing signal instructing data writing, a read instructing signal instructing data reading, a page mode instructing signal instructing a page mode operation, and a precharge instructing signal instructing completion of the page mode operation; and

said signal input circuitry activates said first internal operation instructing signal in accordance with said write instructing signal and said

read instructing signal, activates said second internal operation instructing signal when said page mode instructing signal is active, and activates said third internal operation instructing signal in accordance with said precharge instructing signal.

3. The synchronous semiconductor memory device according to claim 2, wherein

said precharge instructing signal is solely activated.

4. The synchronous semiconductor memory device according to claim 2, wherein

said precharge instructing signal is activated together with one of said write instructing signal and said read instructing signal.

5. The synchronous semiconductor memory device according to claim 1, further comprising:

a mode setting circuit for storing data setting said second internal operation instructing signal to either of a valid state and an invalid state.

6. The synchronous semiconductor memory device according to claim 1, further comprising:

an internal clock producing circuit for producing an internal clock signal having a doubled frequency of said basic clock signal when said second internal operation instructing signal is active, and

said control circuitry activates said column-related circuitry in accordance with said internal clock signal.

7. The synchronous semiconductor memory device according to claim 6, wherein

said internal clock producing circuit produces, as said internal clock signal, a pulse signal of a predetermined time width in response to rising and falling of said basic clock signal when said second internal operation instructing signal is active.

8. The synchronous semiconductor memory device according to claim 6, wherein

said internal clock producing circuit includes

a synchronous clock producing circuit for producing four-phase clock signals of four phases synchronized with said basic clock signal and shifted in phase by a quarter of a cycle period from each other,

a clock combining circuit for producing two-phase clock signals of two phases by combining two clock signals identical in phase and shifted in phase by a quarter of the cycle period for each two clock signals included in said four-phase clock signals of four phases,

a clock control circuit responsive to deactivation of said second internal operation instructing signal, for inhibiting production of a one-phase clock signal of one phase of the two phases of the two-phase clock signals, and

a clock output circuit producing said internal clock signal in accordance with output signals of said clock combining circuit.

9. The synchronous semiconductor memory device according to claim 1, wherein

said control circuitry includes

a row-related activation control circuit for activating said row select circuitry in accordance with said first internal operation instructing signal,

a cycle precharge control circuit for producing a first precharge triggering signal in accordance with a predetermined output control signal of said row-related activation control circuit,

a page precharge control circuit for producing a second precharge triggering signal in accordance with said third internal operation instructing signal,

a trigger switch circuit for selecting one of the first and second precharge triggering signals in accordance with said second internal operation instructing signal, to provide a precharge instruction signal to said row-related activation control circuit, said row-related activation control circuit deactivating said row select circuitry in response to

activation of said precharge instructing signal, and

a column-related activation control circuit for activating and subsequently deactivating said column-related circuitry in response to said predetermined control signal provided from said row-related activation control signal, said second internal operation instructing signal and said first internal operation instructing signal.

10. The synchronous semiconductor memory device according to claim 1, wherein

said plurality of memory cells are is divided into a plurality of banks, and

said control circuitry controls an operation instructed by the internal operation instructing signal provided from said signal input circuitry for a bank designated in accordance with a bank address signal designating the bank.